Track

Sector

Head positioning
RGB electron guns

Pixel

Scan line
Central processing unit (CPU)
Bidirectional data bus

Bus buffers

Chip select

CS

RS 1

Timing and control

RS 0

Register select

I/O read

RD

I/O write

WR

Internal bus

Port A register

I/O data

Port B register

I/O data

Control register

Control lines

Status register

Status lines

To CPU

To I/O device

<table>
<thead>
<tr>
<th>CS</th>
<th>RS1</th>
<th>RS0</th>
<th>Register selected</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
<td>None: data bus in high-impedance state</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Port A register</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Port B register</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Control register</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Status register</td>
</tr>
</tbody>
</table>
(b) Source-initiated transfer
(a) Destination-initiated transfer

(b) Source-initiated transfer
Start bit | Character bits | Stop bits

1 1 0 0 0 1 0 1
Data: 0 0 1 1 0 0 0 1 1 0 1 1 1 1 0

NRZI
### (a) General packet format

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC</td>
<td>Start of packet</td>
<td>8 bits</td>
</tr>
<tr>
<td>PID</td>
<td>Packet ID</td>
<td></td>
</tr>
<tr>
<td>CRP</td>
<td>Checksum</td>
<td></td>
</tr>
<tr>
<td>EOP</td>
<td>End of packet</td>
<td></td>
</tr>
<tr>
<td>Packet Specific Data</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### (b) Output packet

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC</td>
<td>Start of packet</td>
<td>8 bits</td>
</tr>
<tr>
<td>Type</td>
<td>Packet type</td>
<td>4 bits</td>
</tr>
<tr>
<td>Check</td>
<td>Checksum</td>
<td>4 bits</td>
</tr>
<tr>
<td>Device Address</td>
<td>Address of device</td>
<td>7 bits</td>
</tr>
<tr>
<td>Endpoint Address</td>
<td>Address of destination</td>
<td>4 bits</td>
</tr>
<tr>
<td>CRP</td>
<td>Checksum</td>
<td></td>
</tr>
<tr>
<td>EOP</td>
<td>End of packet</td>
<td></td>
</tr>
</tbody>
</table>

### (c) Data packet (Data0 type)

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC</td>
<td>Start of packet</td>
<td>8 bits</td>
</tr>
<tr>
<td>Type</td>
<td>Packet type</td>
<td>4 bits</td>
</tr>
<tr>
<td>Check</td>
<td>Checksum</td>
<td>4 bits</td>
</tr>
<tr>
<td>Data</td>
<td>Data field</td>
<td>Up to 1024 bytes</td>
</tr>
<tr>
<td>CRP</td>
<td>Checksum</td>
<td></td>
</tr>
<tr>
<td>EOP</td>
<td>End of packet</td>
<td></td>
</tr>
</tbody>
</table>

### (d) Handshake packet (Acknowledge type)

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC</td>
<td>Start of packet</td>
<td>8 bits</td>
</tr>
<tr>
<td>Type</td>
<td>Packet type</td>
<td>4 bits</td>
</tr>
<tr>
<td>Check</td>
<td>Checksum</td>
<td>4 bits</td>
</tr>
<tr>
<td>EOP</td>
<td>End of packet</td>
<td></td>
</tr>
</tbody>
</table>
Read status register

Check flag bit

Flag

0

1

Read data register

Transfer data to memory

Operation complete?

No

Yes

Continue program
Interrupt register

Highest priority

3
2
1
0

Lowest priority

Mask register

Interrupt acknowledge from CPU

Priority encoder

A_0

A_1

V

VAD

Interrupt to CPU

Figure 4-12
Bus request → BR
Bus granted ← BG

Address bus → AB
Data bus ← DB
Read ← RD
Write ← WR

High impedance (disabled) if BG = 1
Memory unit

Memory bus

Central processing unit (CPU)

Input-output processor (IOP)

Peripheral devices

I/O bus
CPU operations

Send instruction to test IOP path

If status O.K., send start I/O instruction to IOP

CPU continues with another program

Request IOP status

Check status word for correct transfer

Continue

IOP operations

Transfer status word to memory location

Access memory for IOP program

Conduct I/O transfers using DMA: prepare status report

I/O transfer completed; interrupt CPU

Transfer status word to memory location